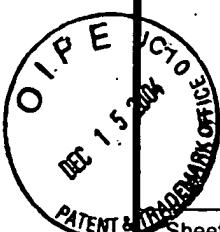


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				Filing Date	05/04/01
				First Named Inventor	Thomas C. McDonald Terry Parks
				Group Art Unit	2188
				Examiner Name	Thang H. Ho GARY PORTKA
Sheet	1	of	2	Attorney Docket Number	CNTR.2063

## U.S. PATENT DOCUMENTS

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Attorney Docket Number	CNTR.2063

## OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
GJP	BA	SAKAMOTO ET AL; <u>Microarchitecture Support for Reducing Branch Penalty in a Superscaler Processor</u> ; pp. 208-216; IEEE 1996; Mitsubishi Electric Corp., System LSI Laboratory, 4-1 Mizuhara, Itami, Hyogo 664, Japan.	
	BB	YEH ET AL; <u>ALTERNATIVE IMPLEMENTATION OF TWO-LEVEL ADAPTIVE BRANCH PREDICTION</u> ; 19 <sup>th</sup> Annual International Symposium on Computer Architecture, pp. 124-134, May 19-21, 1992, Gold Coast, Australia.	
	BC	CHANG ET AL; <u>ALTERNATIVE IMPLEMENTATIONS OF HYBRID BRANCH PREDICTORS</u> ; Proceedings of MICRO-28, 1995, IEEE.	
	BD	MC FARLING, SCOTT; <u>WRL TECHNICAL NOTE TN-36</u> , "Combining Branch Predictors, June 1993, Western Research Laboratory, 250 University Ave., Palo Alto, CA 94301	
	BE	IEEE 100; <u>THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS</u> ; Seventh Edition, IEEE, Standards Information Network, IEEE Press,	
GJP	BF	BRAY ET AL; <u>STRATEGIES FOR BRANCH TARGET BUFFERS</u> ; Technical Report No. CSL-TR-91-480, June 1991.	

Examiner Signature	GARY J. PORTKA	Date Considered	1/18/05
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